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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,016	KEAYS, BRADY L.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-102* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *See Continuation Sheet* is/are rejected.

7)☒ Claim(s) *10,18,22-24,28,34,35,37,42,43,65-67,71,72,77,80-82,96,97,99 and 100* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/25/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims rejected are 1-9,11-17,19-21,25-27,29-33,36,38-41,44-64,68-70,73-76,78,79,83-95,98,101 and 102.

DETAILED ACTION

1. The enclosed detailed action is in response to the Application submitted on January 30, 2004 and the Information Disclosure Statement submitted on August 16, 2004.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 46-62 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 46 and 54 incorporate the language reading one or more user data sectors and/or ECC codes and writing the one or more user data sectors and/or ECC codes. The Examiner was not able to find any description in the specification to enable the and/or claimed features. Clarification is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6, 29-32, 38-40, 44, 67, 69-70, 73-74, 85-88, 93-95, 98 and 101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri (USPN: 6,262,918) in view of Iwata et al (PGPUB: US 2004/0193774) and Harper (USPN: 4,918,600).

Regarding claims 1, 29, 44, 69, 85, 93-95 and 101, Estakhri discloses at least one non-volatile memory device, wherein the at least one non-volatile memory device contains a memory array with a plurality of physical row pages (sectors) arranged in a plurality of erase blocks, wherein each physical row page containing one or more user data sectors and one or more overhead data areas (Abstract); Estakhri does not disclose a non-split data move control circuit adapted to move one or more selected user data sectors and associated overhead data areas stored in one or more physical row pages of a selected source erase block to a target erase block in a modified copy back move operations such that selected user data sectors and the associated overhead data areas stored in a source physical row page of the source erase block are moved to a target physical row page of the target erase block by reading the selected user data sectors and the associated overhead areas into an internal latch of the at least one non-volatile memory device; transferring the selected data from the selected non-volatile memory device; masking the selected user data sectors and the associated overhead data areas and writing the selected data to a physical page row of a target erase block. However, Iwata discloses a non-split data move control circuit (circuitry responsible for performing merge operations) adapted to move one or more selected user data sectors and associated overhead data areas stored in one or more physical row pages of a selected source erase block to a target erase block in a modified copy back move operations (merge operation) such that selected user data sectors and the associated overhead data areas stored in a source physical row page of the source erase block are moved to a target physical row

page of the target erase block by reading the selected user data sectors and the associated overhead areas (data) into an internal latch (Figure 1, Reference 4a) of the at least one non-volatile memory device (section 0028, lines 2-4; section 0153; section 0132); transferring the selected data from the selected non-volatile memory device and writing the selected data to a physical page row of a target erase block (section 0028, lines 4-10; section 0132). The features taught by Iwata provide an increase in the amount of available storage (section 0017). Iwata does not disclose masking off a first selected range of column bit values. However, Harper teaches the concept of selecting a portion of data by masking the data (C 14, L 38-47). This feature taught by Harper provides efficiency by allowing the system to specifically extract the data needed or desired from the remaining data. In Iwata's system the entire read data is transferred and written into a target block. However, in other situations it may be desirable to write portions of the read data and not the entire amount of data read. One of ordinary skill in the art would have been motivated to use the teachings of Iwata and Harper (to allow the system to write portions of data by masking) in the system taught by Estakhri for the desirable purpose of efficiency and flexibility.

Regarding claims 2, 31, 39, 74, 86, 88 Estakhri, Iwata and Harper disclose a mass storage device compatible interface to the non-volatile memory system (Estakhri, C 1, L 19-40; Iwata, sections 0002 and 0003).

Regarding claim 3, Estakhri, Iwata and Harper disclose the non-volatile memory system having a PCMCIA-ATA compatible interface (Estakhri, C 4, L 41-43).

Regarding claims 4, 30, 38 and 70 Estakhri, Iwata and Harper disclose a NAND architecture Flash memory device (Iwata, section 0095).

Regarding claim 5, Estakhri, Iwata and Harper disclose the user data sector containing 512 bytes (Estakhri, C 2, L 61-64).

Regarding claims 6, 32, 40 Estakhri, Iwata and Harper discloses each overhead data area containing an error correction code (ECC)(Estakhri, C 2, L 40-42).

Regarding claims 67, 73 and 98, Estakhri, Iwata and Harper do not disclose making out a selected range of data by inserting logical l's. However, it is well known in the art to perform masking by inserting logical 1's and such functionality is a simple mechanism for masking out data. Thus it would have been obvious to one of ordinary skill in the art to mask out the selected bits in the system taught by Estakhri, Iwata and Harper by inserting logical 1's for the desirable purpose of simplicity.

Regarding claim 87, Estakhri, Iwata and Harper disclose the host comprising a processor and external memory controller (Estakhri, C 4, L 14-15).

6. Claims 7, 33, 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri (USPN: 6,262,918) in view of Iwata et al (PGPUB: US 2004/0193774) and Harper (USPN:

4,918,600) as applied to claim 1 above and further in view of Miura (PGPUB: US 20060041711).

Estakhri, Iwata and Harper disclose ECC codes but they do not explicitly disclose evaluating the ECC codes as data is moved. Miura discloses evaluating ECC codes as data is being moved (section 0111). This feature taught by Miura provides reliability by ensuring that the data moved is accurate. Hence, it would have been obvious to one of ordinary skill in the art to evaluate the ECC codes as the data is moved in the system taught by Estakhri, Iwata and Harper for the desirable purpose of reliability.

7. Claims 8-9, 11-14, 16-17, 20-21, 25-26, 36, 45, 75-76, 78, 84, 89-92 and 102 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri (USPN: 6,262,918) in view of Iwata et al (PGPUB: US 2004/0193774) and Gonzalez (USPN: 7,032,065).

Regarding claims 8-9, 16-17, 20-21, 25, 36, 45, 75-76, 84, 89 and 102, Estakhri discloses at least one non-volatile memory device, wherein the at least one non-volatile memory device contains a memory array with a plurality of physical row pages (sectors) arranged in a plurality of erase blocks, wherein the blocks of the at least one non-volatile memory device are arranged in pairs into a plurality of superblocks and each physical row page containing one or more user data sectors and one or more overhead data areas (Abstract). Estakhri does not disclose a split data move control circuit adapted to move one or more selected user data sectors stored in two or more physical row pages of a selected source super block to a target super block such that the selected user data sectors stored in a first source physical row page of the source super block are moved to a first target physical row page of the target super block and the associated overhead

data areas of the selected user data sectors stored in a second source physical row page of the source super block are moved to a second target physical row page of the target super block. However, Iwata teaches the concept of moving source blocks, which contain plurality of pages, to a target block (section 0028, lines 2-10; section 0153). This feature taught by Iwata provides an increase in the amount of available storage (section 0017). Iwata does not explicitly disclose storing the user data and the overhead data in different rows/pages/blocks. Gonzalez teaches the concept of storing the user data and overhead data in different sector/pages/row/blocks/memories (C 3, L 48-57; C 8, L 34-54). This feature taught by Gonzalez provides efficiency by providing effective utilization of the storage capacity of the pages/blocks (C 3, L 6-26). Hence, one of ordinary skill in the art would have been motivated to incorporate the teachings of Iwata and Gonzalez to the system taught by Estakhri for the desirable purpose of efficiency.

Regarding claims 11, 90 and 92, Estakhri, Iwata and Gonzalez disclose a mass storage device compatible interface to the non-volatile memory system (Estakhri, C 1, L 19-40; Iwata, sections 0002 and 0003).

Regarding claim 12, Estakhri, Iwata and Gonzalez disclose the non-volatile memory system having a PCMCIA-ATA compatible interface (Estakhri, C 4, L 41-43).

Regarding claims 13 and 26, Estakhri, Iwata and Gonzalez disclose a NAND architecture Flash memory device (Iwata, section 0095).

Regarding claims 14 and 78, Estakhri, Iwata and Gonzalez disclose each overhead data area containing an error correction code (ECC)(Estakhri, C 2, L 40-42).

Regarding claim 91, Estakhri, Iwata and Gonzalez disclose the host comprising a processor and external memory controller (Estakhri, C 4, L 14-15).

8. Claims 15, 19, 27, 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri (USPN: 6,262,918) in view of Iwata et al (PGPUB: US 2004/0193774) and Gonzalez (USPN: 7,032,065) as applied to claim 8 above and further in view of Miura (PGPUB: US 20060041711).

Estakhri, Iwata and Gonzalez disclose ECC codes but they do not explicitly disclose evaluating the ECC codes as data is moved. Miura discloses evaluating ECC codes as data is being moved (section 0111). This feature taught by Miura provides reliability by ensuring that the data moved is accurate. Hence, it would have been obvious to one of ordinary skill in the art to evaluate the ECC codes as the data is moved in the system taught by Estakhri, Iwata and Gonzalez for the desirable purpose of reliability.

9. Claims 63-64, 68 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al (PGPUB: US 2004/0193774) in view of Harper (USPN: 4,918,600).

Iwata discloses reading data of a physical page row of a source erase block from a selected non-volatile memory device of one or more non-volatile memory devices (section 0028, lines 2-4;

section 0153); transferring the selected data from the selected non-volatile memory device and writing the selected data to a physical page row of a target erase block (section 0028, lines 4-10). Iwata does not disclose masking off a first selected range of column bit values. However, Harper teaches the concept of selecting a portion of data by masking the data (C 14, L 38-47). This feature taught by Harper provides efficiency by allowing the system to specifically extract the data needed or desired from the remaining data. In Iwata's system the entire read data is transferred and written into a target block. However, in other situations it may be desirable to write portions of the read data and not the entire amount of data read. One of ordinary skill in the art would have been motivated to allow the system to write portions of data and would have been motivated to use Harper's teachings to implement the feature for the desirable purpose of flexibility and efficiency.

Regarding claims 64, Iwata and Gonzalez disclose a NAND architecture Flash memory device (Iwata, section 0095).

Regarding claim 68, Iwata and Gonzalez disclose a mass storage device compatible interface to the non-volatile memory system (Iwata, sections 0002 and 0003).

Allowable Subject Matter

10. Claims 46-62 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 1st paragraph, set forth in this Office action.

11. Claims 10, 18, 22-24, 28, 34-35, 37, 42-43, 65-67, 71-72, 77, 80-82, 96-97, 99-100 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 571-272-4194. The examiner can normally be reached on Mon, Wed, Thurs (10-4), Tues (9:45 - 6:15).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

Kimberly N. McLean-Mayo
Primary Examiner
Art Unit 2187

KNM

June 26, 2006